Notice of Allowability	Application No.	Applicant(s)	
	10/608,320	WENG ET AL.	
	Examiner	Art Unit	
	Mujtaba K. Chaudry	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *interview on June 27, 2007*.

2. ☒ The allowed claim(s) is/are *1-3 and 5-28*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *6/27/2007* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

GUY LAMARRE
PRIMARY EXAMINER

6/27/07

EXAMINER'S AMENDMENT

An Examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this Examiner's amendment was given in a telephone interview with Patricia A. Sheehan on Wednesday, June 27, 2007.

Please further amend the application as follows:

Please replace claim 1 with:

1. A method of decoding errors occurring in data stored in memory, comprising:

applying data to be stored in a buffer memory as a plurality of data words to a generator matrix to generate a set of parity check bits;

storing the plurality of data words in a plurality of data buffer locations in the buffer memory and the set of parity check bits in one or more parity check buffer locations in the buffer memory, the parity check buffer locations being different locations than the data buffer locations that contain the data;

reading all of the stored data words and the set of parity check bits from the respective data buffer and parity check buffer locations;

regenerating the set of parity check bits for all of the data words; and

producing from all of the stored and the set of regenerated parity check bits a result that is usable to directly identify:

i. the data buffer location that contains a data word with an erroneous bit and

ii. the position of the erroneous bit in the data word contained in the identified data buffer location.

Please replace claim 23 with:

23. An encoding method comprising:

applying data to be stored in a buffer memory to a generator matrix as a plurality of data words to generate a set of parity check bits for all the data words;

wherein the generator matrix comprises a data portion and a parity check generation portion, and the parity check generation portion comprises rows of bits corresponding to binary representations of respective data buffer locations to be used to store all of the data words;

storing all of the data words in the buffer memory at the data buffer locations; and

storing the set of parity check bits in one or more parity check locations of the buffer memory, the parity check locations being different locations than the data buffer locations that contain the data.

Please replace claim 24 with:

24. A data storage system comprising:

a storage medium;

a controller coupled to the storage medium; and

a buffer memory coupled to the storage medium and the controller for storing data to be written to the storage medium and data read from the storage medium;

wherein the controller is operable to perform the following steps:

applying data to be stored in a buffer memory as a plurality of data words to a generator matrix to generate a set of parity check bits;

storing all of the data words in a plurality of data buffer locations and the set of parity check bits in one or more parity check buffer locations of the buffer memory, the parity check buffer locations being different than the data buffer locations that contain the data;

reading all of the stored data words and the set of parity check bits;

regenerating the set parity check bits for all of the data words; and

producing from all of the stored data words and all of the regenerated parity check bits a result that is usable to directly identify:

i. a data buffer location that contains a data word with an erroneous bit, and

ii. the position of the erroneous bit in the data word.

Please replace claim 25 with:

25. A data storage system comprising:

a storage medium;

a controller coupled to the storage medium; and

a buffer memory coupled to the storage medium and the controller for storing data to be written to the storage medium and data read from the storage medium;

wherein the controller is operable to perform the following steps:

applying data to be stored in the buffer memory as a plurality of data words to a generator matrix to generate a set of parity check bits for all the data words, the generator matrix comprising a data portion and a parity check generation portion;

the parity check generation portion comprises rows of bits corresponding to binary representations of the respective data buffer locations to be used to store the data;

storing all of the data words in the buffer memory at the data buffer locations; and

storing the set of parity check bits in the buffer memory in one or more parity check buffer locations that are different than the data buffer locations that contain the data.

Please replace claim 26 with:

26. An apparatus comprising:

a controller coupled to a storage medium; and

a buffer memory coupled to the controller for storing data to be written to the storage medium and data read from the storage medium;

wherein the controller is operable to perform the following steps:

applying data to be stored in a buffer memory as a plurality of data words to a generator matrix to generate a set of parity check bits;

storing all of the data words in respective data buffer memory locations and the set parity check bits in one or more parity check buffer locations that are different locations than the data buffer locations that contain the data;

reading all of the stored data words and the set of parity check bits;

regenerating the set of parity check bits for all of the data words; and

producing from all of the stored data words and the set of regenerated parity check bits a result that is usable to directly identify:

i. a data buffer location of a data word that contains an erroneous bit and

ii. the position of the erroneous bit in the data word.

Please replace claim 27 with:

27. An apparatus comprising:

a controller coupled to a storage medium; and

a buffer memory coupled to the controller for storing a plurality of data words to be written to the storage medium and read from the storage medium;

wherein the controller is operable to perform the following steps:

applying all of the data words to be stored in a plurality of addressable data buffer locations in the buffer memory to a generator matrix to generate a set of parity check bits, the generator matrix comprising a data portion and a parity check generation portion;

wherein the parity check generation portion comprises rows of bits corresponding to binary representations of the data buffer locations to be used to store all of the data words;

storing all of the data words in the buffer memory at the addressable data buffer locations; and

storing the set of parity check bits in the buffer memory in one or more addressable parity check buffer locations that have are different addresses than the data buffer locations that contain all of the data words.

Please replace claim 28 with:

28. An apparatus comprising:

a controller coupled to a storage medium; and

a buffer memory coupled to the controller for storing a plurality of data words to be written to the storage medium and read from the storage medium, the buffer memory including separately addressable multiple symbol storage locations;

wherein the controller is operable to perform the following steps:

applying all of the data words to a generator matrix to generate a set of parity check bits, the generator matrix including a parity check generation portion that includes rows of bits that correspond to the addressable storage locations to be used to store the data;

storing all of the data words in the corresponding addressable storage locations as a plurality of data words;

storing the set of parity check bits generated by the generator matrix in storage locations that are addressable separately from the storage locations in which the data words are stored;

retrieving all of the data words and the set of parity check bits from their respective storage locations and regenerating the set of parity check bits; and

producing from the stored and regenerated parity check bits a result that is usable to directly identify:

i. the addressable storage location that contains a data word with an erroneous bit, and

ii. the position of the erroneous bit in the data word contained in the identified storage location.

REASONS FOR ALLOWANCE

Claims 1-3 and 5-28 are allowed. The following is an Examiner's statement of reasons for allowance:

Independent claim 1 of the present application teaches, for example, a method of decoding errors occurring in data stored in memory, comprising: applying data to be stored in a buffer memory as a plurality of data words to a generator matrix to generate a set of parity check bits; storing the plurality of data words in a plurality of data buffer locations in the buffer memory and the set of parity check bits in one or more parity check buffer locations in the buffer memory, the parity check buffer locations being different locations than the data buffer locations

that contain the data; reading all of the stored data words and the set of parity check bits from the respective data buffer and parity check buffer locations; regenerating the set of parity check bits for all of the data words; and producing from all of the stored and the set of regenerated parity check bits a result that is usable to directly identify: i. the data buffer location that contains a data word with an erroneous bit and ii. the position of the erroneous bit in the data word contained in the identified data buffer location. The foregoing limitations are not found in the prior arts of record. Particularly, none of the prior arts of record teach nor fairly suggest, "...applying data to be stored in a buffer memory as a *plurality of data words to a generator matrix to generate a set of parity check bits*; storing the plurality of data words in a plurality of data buffer locations in the buffer memory and the set of parity check bits in one or more parity check buffer locations in the buffer memory, *the parity check buffer locations being different locations than the data buffer locations that contain the data*; *reading all of the stored data words and the set of parity check bits from the respective data buffer and parity check buffer locations*; regenerating the set of parity check bits for all of the data words; and producing from all of the stored and the set of regenerated parity check bits a result that is usable to directly identify: i. the data buffer location that contains a data word with an erroneous bit and ii. the position of the erroneous bit in the data word contained in the identified data buffer location."

Independent claims 23-28 include similar limitations of independent claim 1 and therefore are allowed for similar reasons.

Dependent claims 2, 3 and 5-22 depend from allowable independent claim1 and inherently include limitations therein and therefore are allowed as well.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mujtaba K. Chaudry whose telephone number is 571-272-3817. The examiner can normally be reached on Mon-Fri 9-7:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on 571-272-6962.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mujtaba Chaudry
Art Unit 2112
June 27, 2007

GUY LAMARRE
PRIMARY EXAMINER